Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **N. CLEAR**
2. **Q1**
3. **D1**
4. **D2**
5. **Q2**
6. **D3**
7. **Q3**
8. **VSS**
9. **CLK**
10. **Q4**
11. **D4**
12. **Q5**
13. **D5**
14. **D6**
15. **Q6**
16. **VDD**

**.073”**

**14**

**13**

**12**

**11**

**2 1 16 15**

**3**

**4**

**5**

**6**

**7 8 9 10**

**MASK**

**REF**

**10276**

**.083”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004 x .004”**

**Backside Potential: VDD**

**Mask Ref: 10276**

**APPROVED BY: DK DIE SIZE .073” X .083” DATE: 10/20/21**

**MFG: HARRIS / RCA THICKNESS .020” P/N: CD40174B**

**DG 10.1.2**

#### Rev B, 7/1